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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,741	07/30/2003	Woong-Kwon Kim	053785-5124	8912

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EXAMINER	
WANG, GEORGE Y	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,741	KIM ET AL.	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 3-17, and 19-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munakata et al. (U.S. Patent No. 6,373,540, hereinafter "Munakata") in view of Ohta et al. (U.S. Patent No. 6,208,399, hereinafter "Ohta").

3. As to claims 1 and 17, Munakata discloses the a liquid crystal display (LCD) device (fig. 1a, 1b) and method having COT structure array substrate comprising a top

gate type thin film transistor (TFT) (col. 7, lines 9-12) formed on a substrate (fig. 1a, ref. 2), an active layer (fig. 1a, ref. 18), a gate electrode (fig. 1a, ref. 16), a source electrode (fig. 1a, ref. 21), and a drain electrode (fig. 1a, ref. 22), a storage capacitor electrode (fig. 1a, ref. Cs), a black matrix (fig. 1a, ref. BM) on top of the TFT, a first pixel electrode (fig. 1a, ref. 9b) contacting the drain electrode (fig. 1a, ref. 22), a color filter (fig. 1a, ref. 14; col. 5, lines 6-8) on the first pixel electrode, and a second pixel electrode (fig. 1a, ref. 11) at a portion over the black matrix.

However, the reference fails to specifically disclose a storage capacitor having a first storage electrode.

Ohta discloses an LCD device having a storage capacitor having a first storage electrode (fig. 4, ref. Cstg).

It would have been obvious to one ordinary skill in the art at the time the invention was made to have a first storage electrode as part of a two-electrode storage capacitor since one would be motivated to minimize the parasitic capacitance in order to maximize storage of information written in the pixels for a long period time (col. 16, lines 18-20). Furthermore, storage capacitance of this type also works to reduce the influence produced by a change in the gate potential (col. 15, lines 32-38). This ultimately serves to reduce the so-called sticking phenomenon which retains a previous image at the time of switching the LCD screen (col. 16, lines 50-53).

4. Regarding claims 3-6 and 19-22, Munakata discloses the LCD device and method as recited above further comprising a gate insulation layer (fig. 1a, ref. 17)

between the active layer and the gate electrode, an interlayer insulator (fig. 1a, ref. 20a) covering the gate and the second storage electrode, and where the insulation layers have contact holes exposing portions of the active layer (col. 6, lines 34-40).

5. As to claims 7-9 and 23-25, Munakata discloses the LCD device and method as recited above further comprising a passivation layer (fig. 1a, ref. 20b) formed beneath the pixel electrode with a third contact hole exposing a portion of the drain electrode on the drain electrode and the black matrix (col. 42-49).

6. As per claims 10-14 and 26-30, Munakata discloses the LCD device and method as recited above where the black matrix is formed of insulating black resin (col. 5, lines 13-20), the active layer has an L-shape (fig. 1b, 18), and where the active layer is formed of a polycrystalline silicon (col. 6, lines 28-29) that is doped except for a portion corresponding to the gate electrode by using stoppers (col. 7, lines 2-8).

7. Regarding claims 15 and 31, Munakata discloses the LCD device and method as recited above, however, the reference fails to specifically disclose a storage capacitor electrode that is connected to the active layer as a single layer.

Ohta discloses an LCD device having a storage capacitor having a first storage electrode (fig. 4, ref. Cstg) that is connected to the active layer (fig. 3, ref. AS) as a single layer.

It would have been obvious to one ordinary skill in the art at the time the invention was made to have a first storage electrode that is connected to the active layer as a single layer since one would be motivated to minimize the parasitic capacitance in order to maximize storage of information written in the pixels for a long period time (col. 16, lines 18-20). Furthermore, storage capacitance of this type also works to reduce the influence produced by a change in the gate potential (col. 15, lines 32-38). This ultimately serves to reduce the so-called sticking phenomenon which retains a previous image at the time of switching the LCD screen (col. 16, lines 50-53).

8. As to claims 16 and 32, Munakata discloses the LCD device and method as recited above where the second storage electrode (fig. 1a, ref. Cs) is parallel to the gate line.

9. As per claim 33, Munakata discloses the LCD device and method as recited above where forming the first and second pixels comprises depositing a first and second conductive layer and patterning them at the same time (fig. 3a-3c).

10. Claims 2 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munakata and Ohta, in further view of Hwang (U.S. Patent No. 6,545,730).

Munakata, when modified by Ohta, discloses the LCD device and method as recited above, however, the reference fails to specifically disclose a buffer layer between the top gate type TFT and the substrate.

Hwang discloses an LCD device having a buffer layer (fig. 2, ref. 20) between the top gate type TFT and the substrate.

It would have been obvious to one of ordinary skill in the art at the invention was made to have included a buffer layer between the top gate type TFT and the substrate since one would be motivated to protect the source and drain regions of doped polysilicon from over-etching, ultimately to prevent impurities of the lower insulating substrate from contaminating other layers (col. 2, lines 29-34).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
December 3, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER